

TITLE: A MULTI-PAIR GIGABIT TRANSCEIVER  
INVENTOR: AGAZZI  
APPLICATION NO.: UNASSIGNED,  
CONF. NO. ; DOCKET NO. 13469US03  
ATTORNEY: JAW, PHONE: 312-775-8000

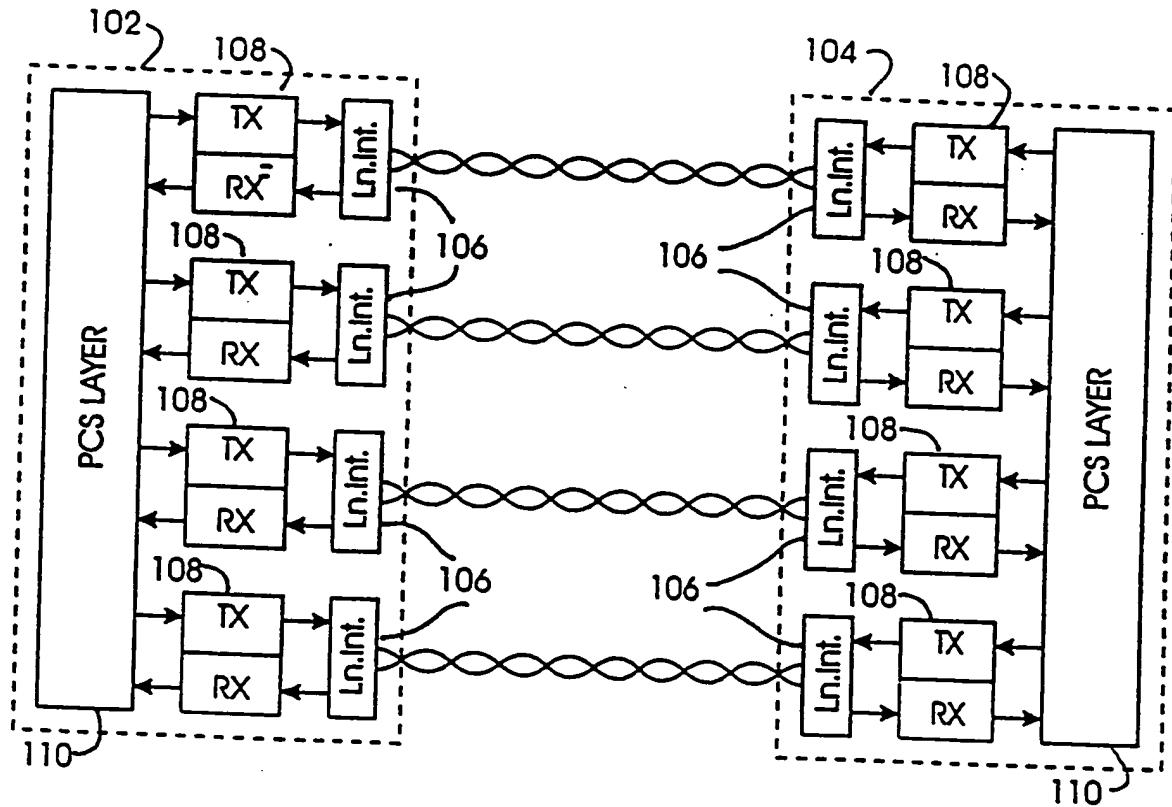


FIG. 1

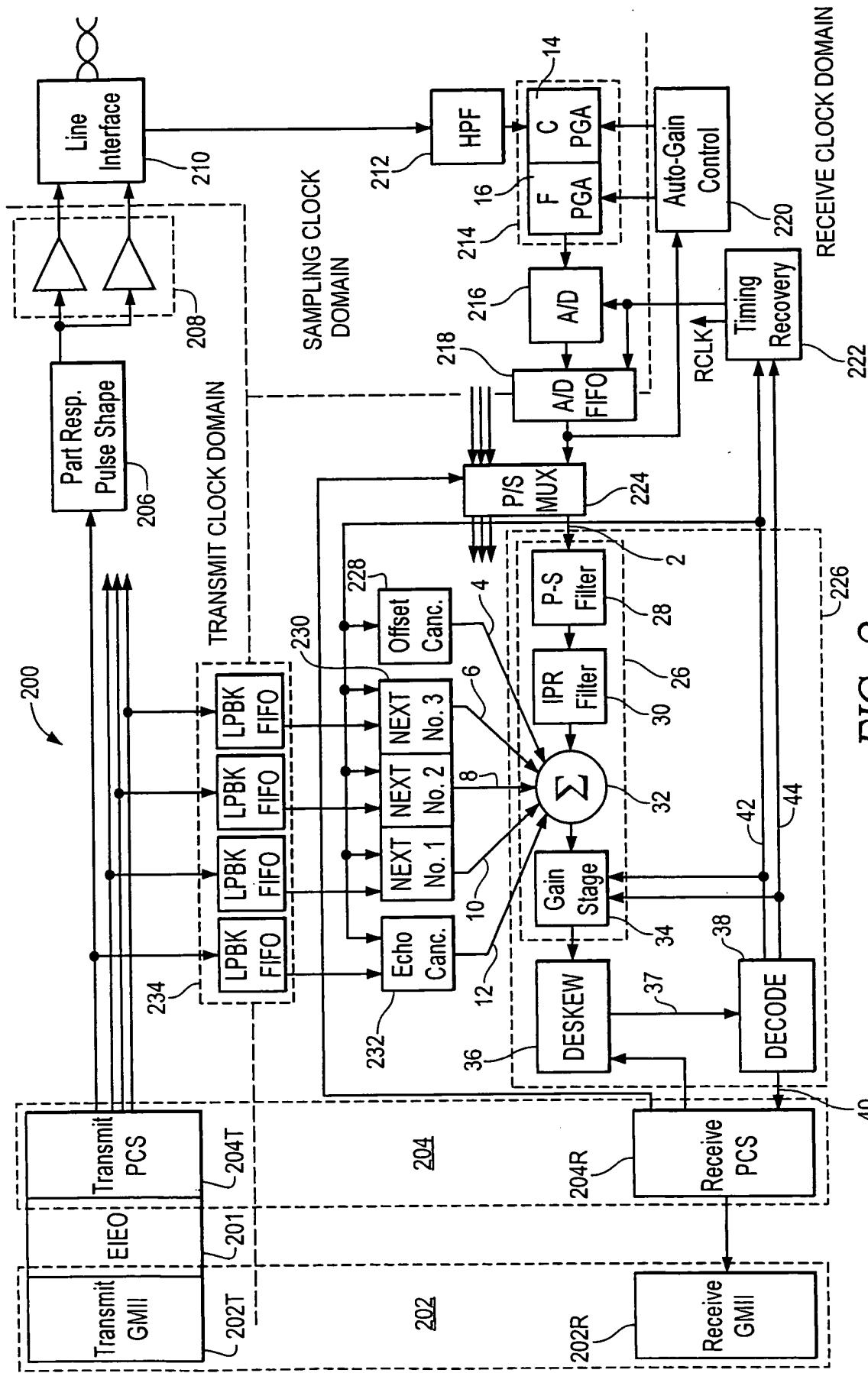


FIG. 2

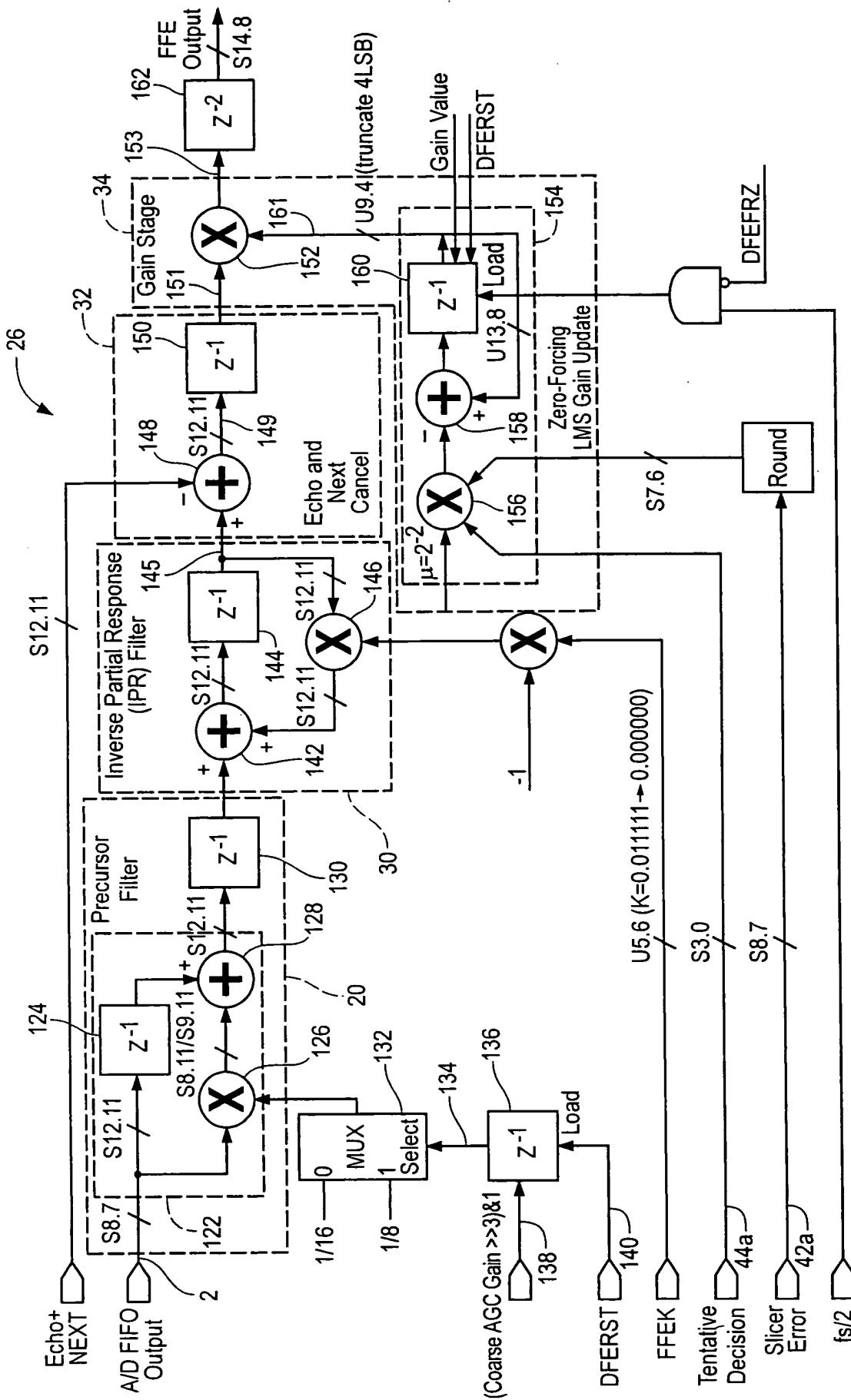


FIG. 2A

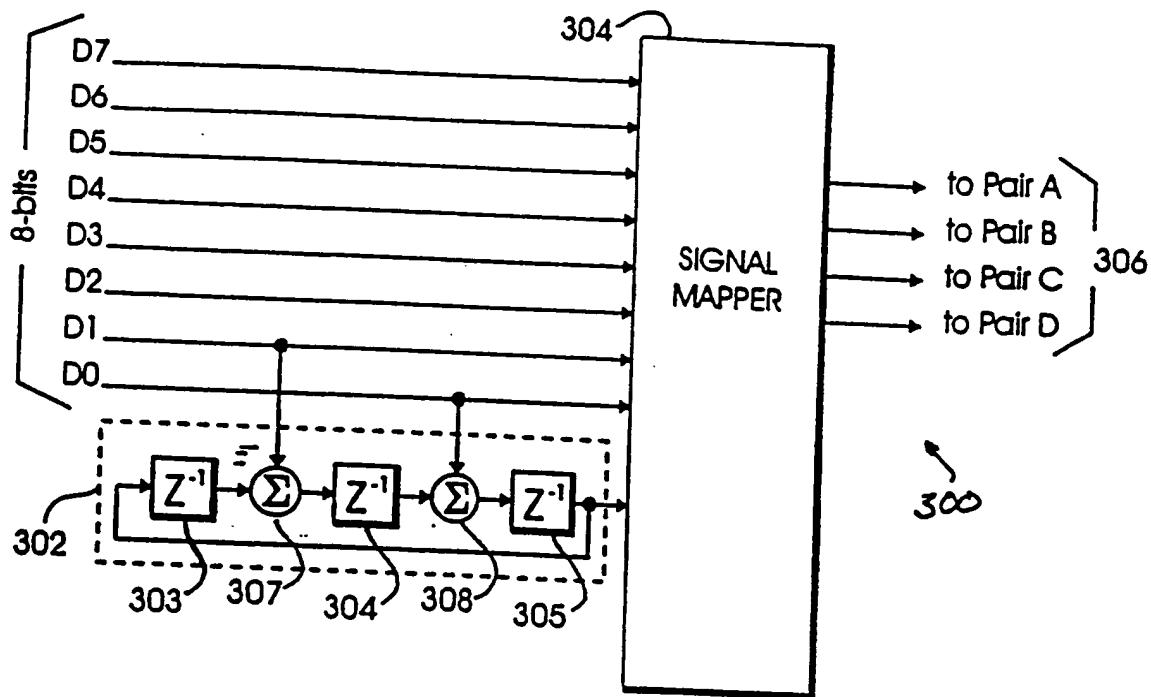


FIG. 3

	Pair ABCD	Pair ABCD
s0	XXXX	U YYY
s1	XXYY	U YYX
s2	XXYY	U YYXX
s3	XXYY	U YYXY
s4	XYXX	U YXXY
s5	XYYY	U YXXX
s6	XYXY	U YXYX
s7	XYXX	U YXYY

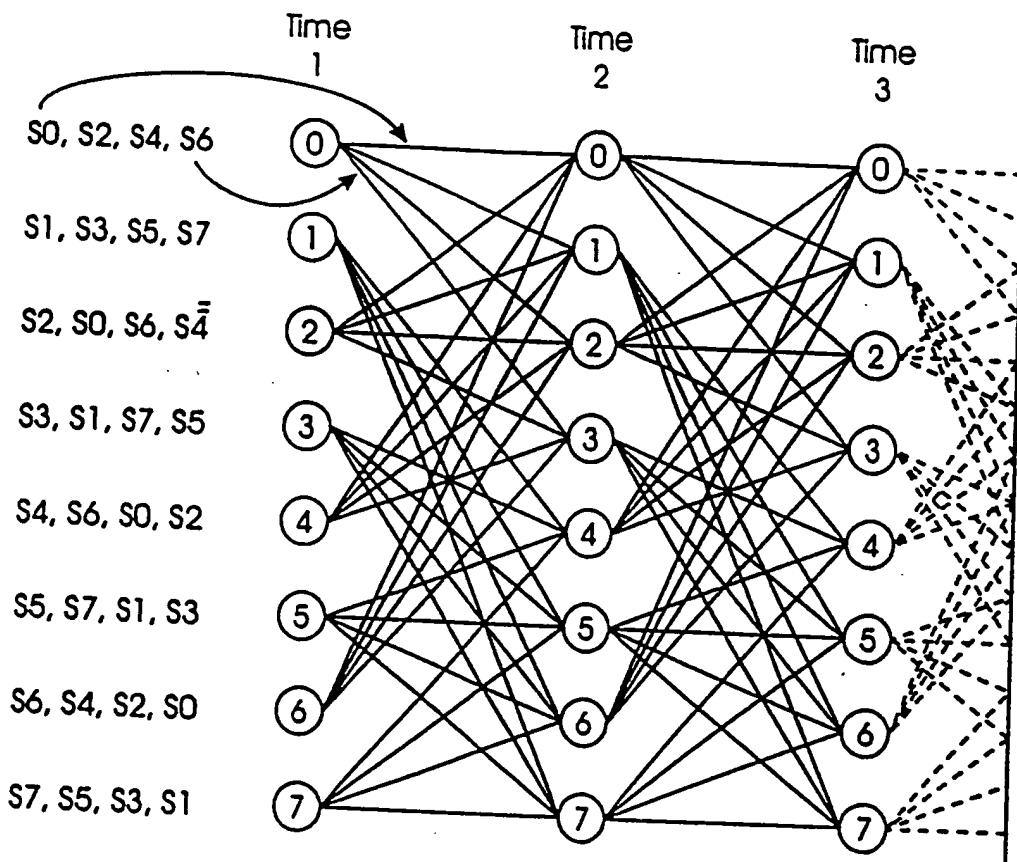
Diagram illustrating the mapping of 8-bit input states (s0-s7) to four-bit patterns for four pairs (ABCD). The patterns are mapped as follows:

- s0: XXXX, U, YYY
- s1: XXYY, U, YYX
- s2: XXYY, U, YYXX
- s3: XXYY, U, YYXY
- s4: XYXX, U, YXXY
- s5: XYYY, U, YXXX
- s6: XYXY, U, YXYX
- s7: XYXX, U, YXYY

Y and X are binary digits, and U is a symbol representing a neutral state.

FIG. 4A

FIG. 4B



*FIG. 5*

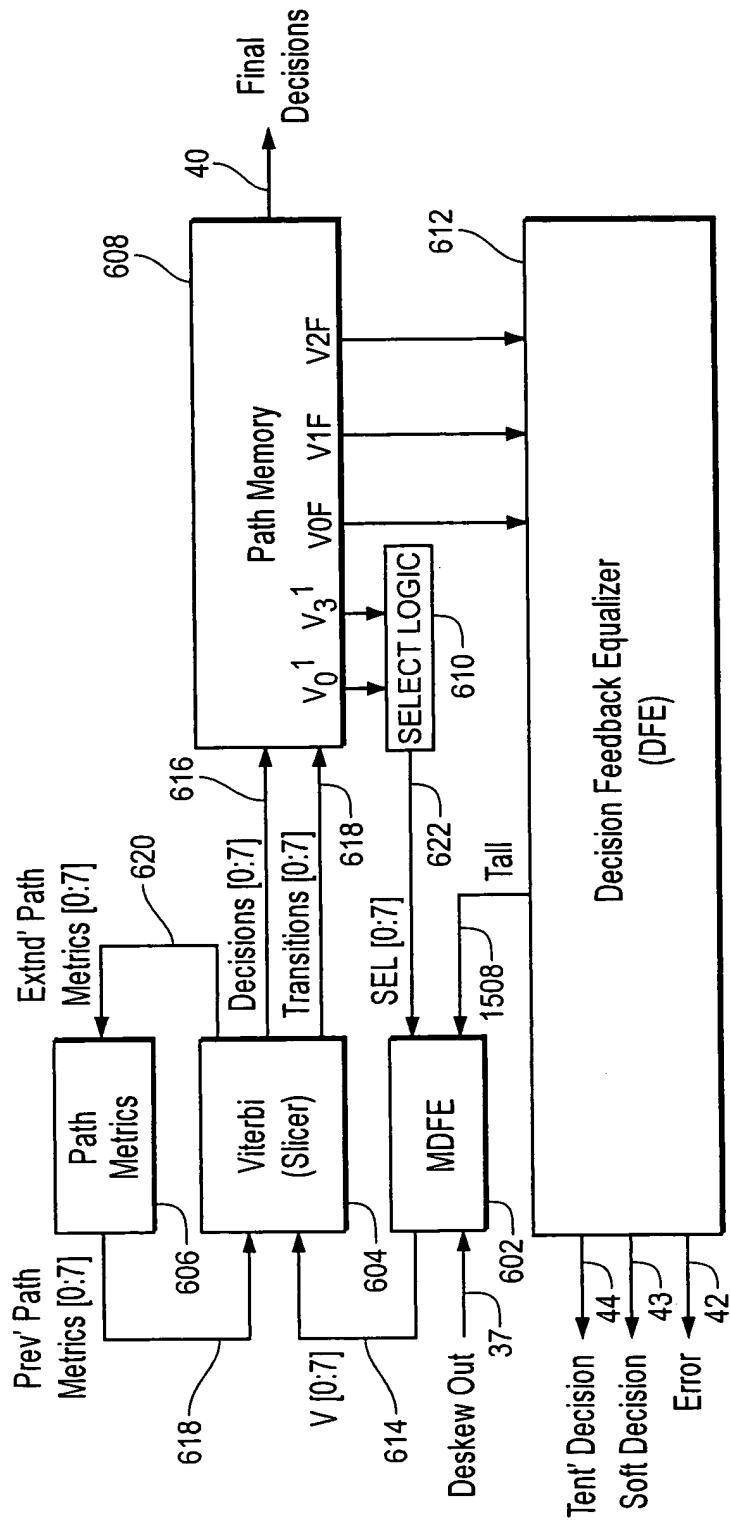


FIG. 6

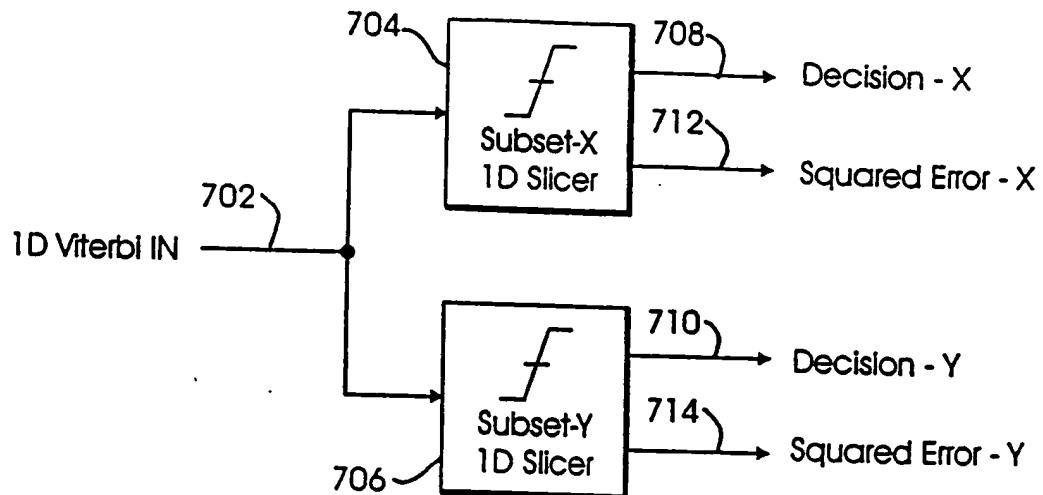


FIG. 7

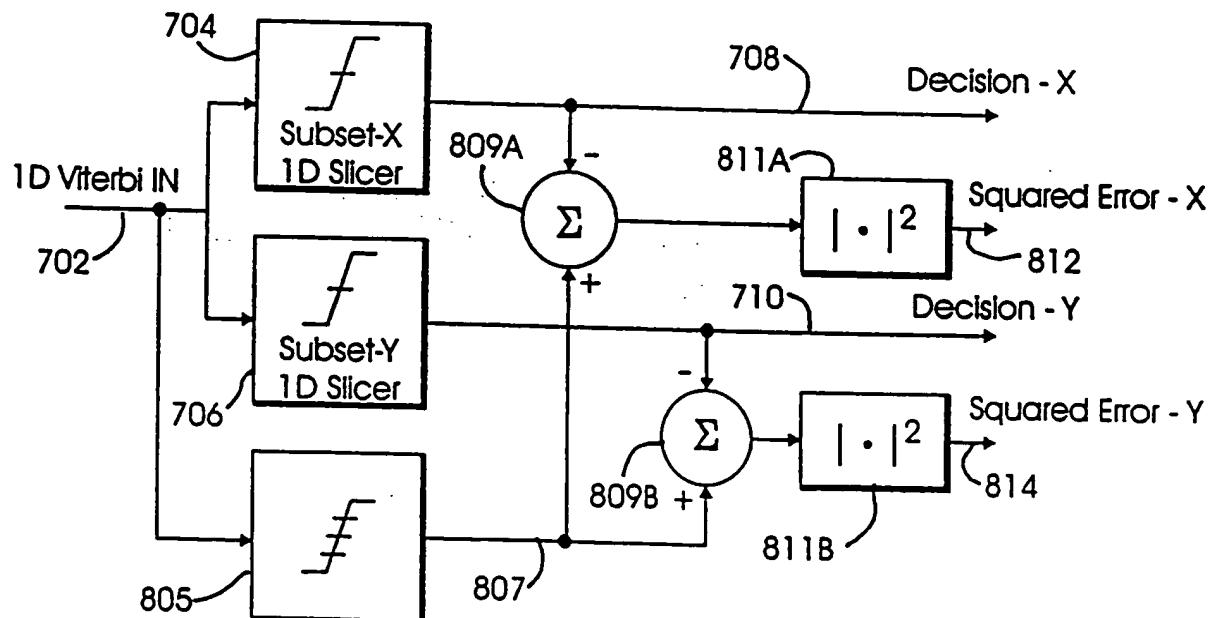


FIG. 8

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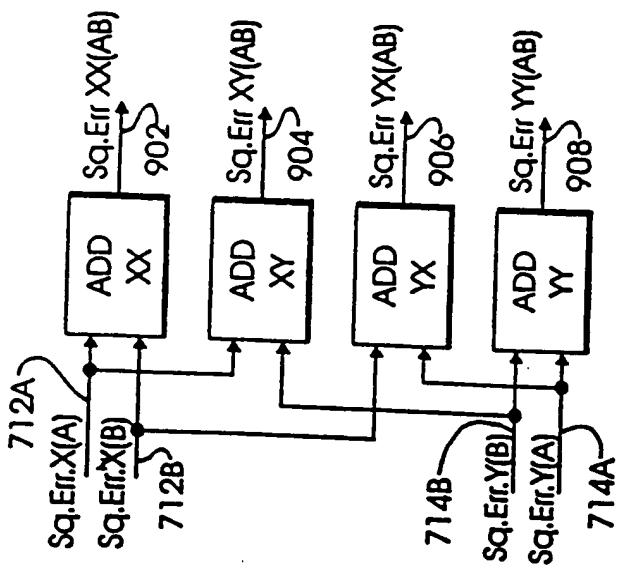


FIG. 9

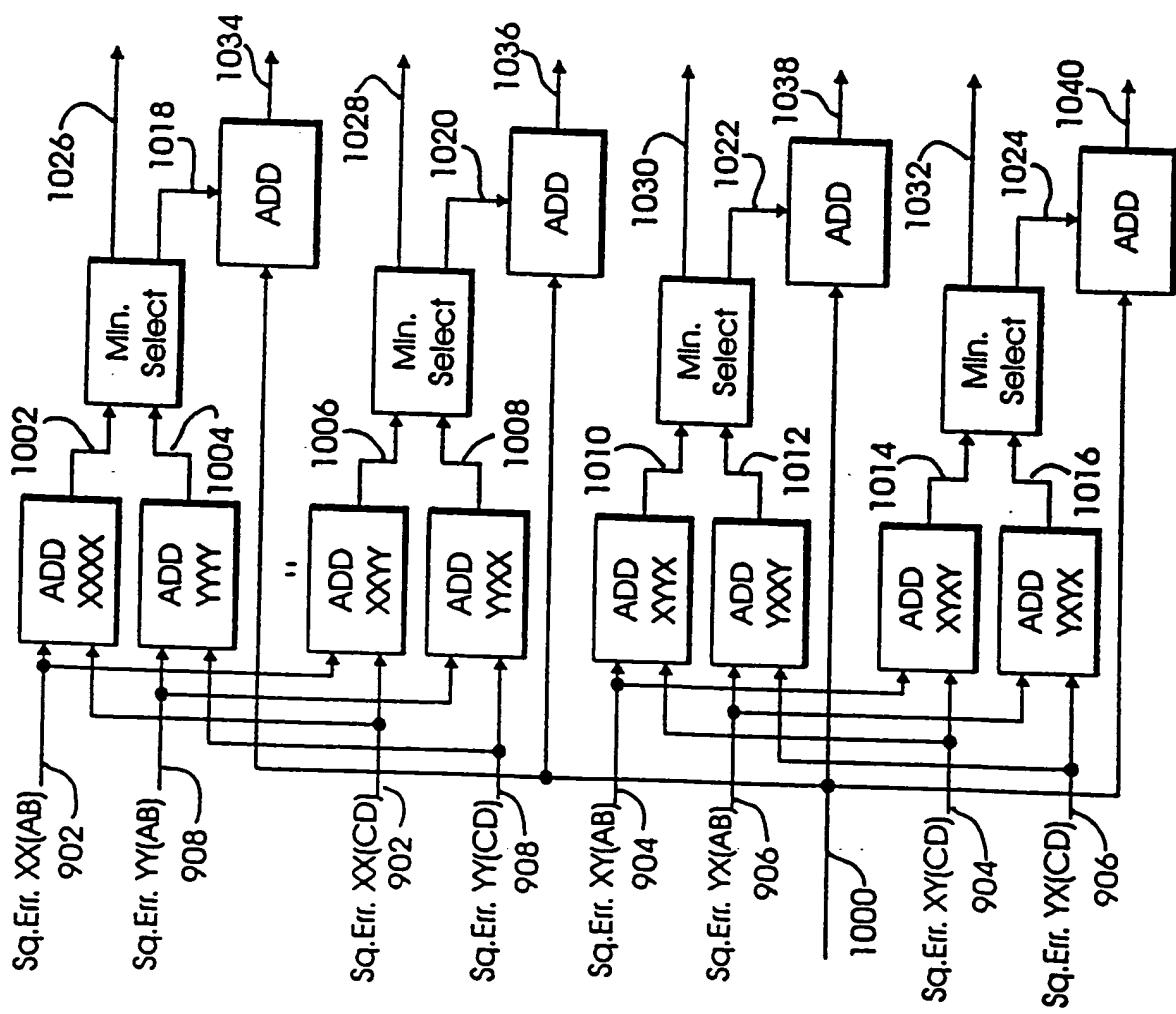


FIG. 10

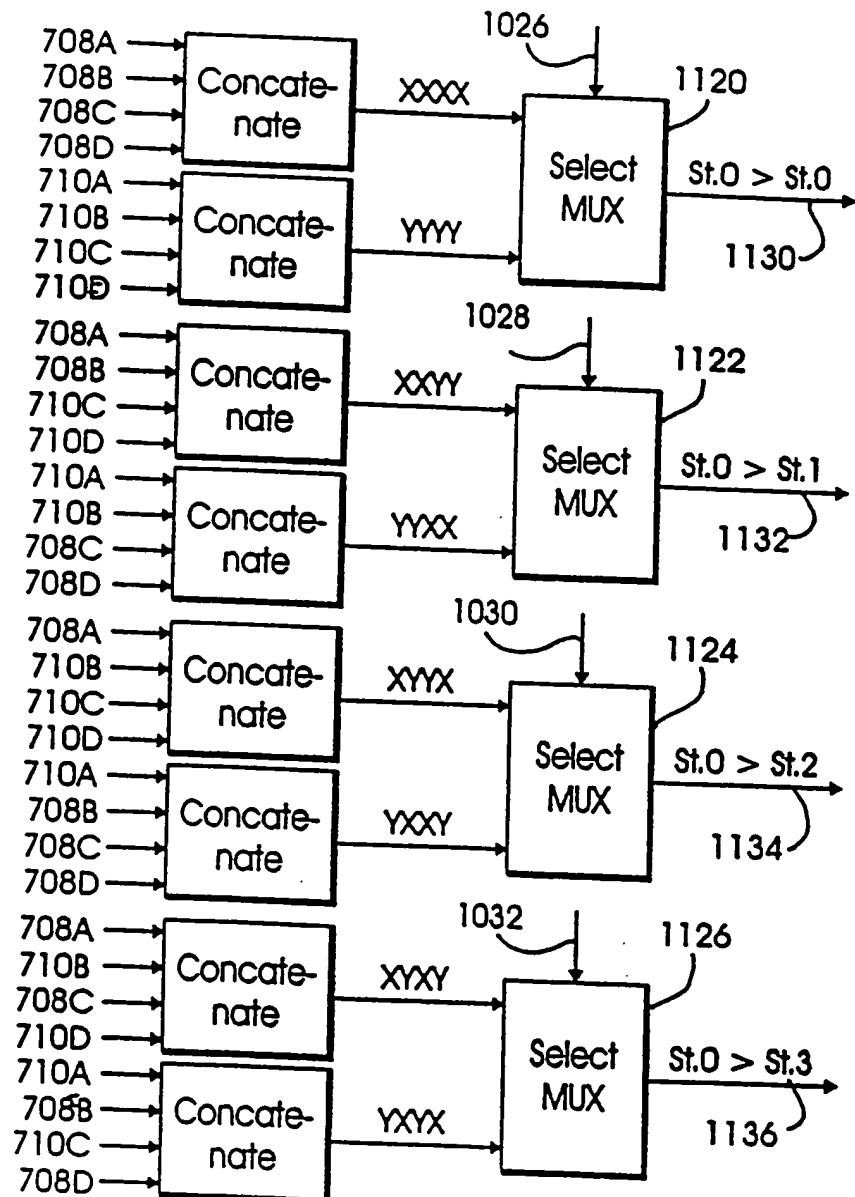


FIG. 11

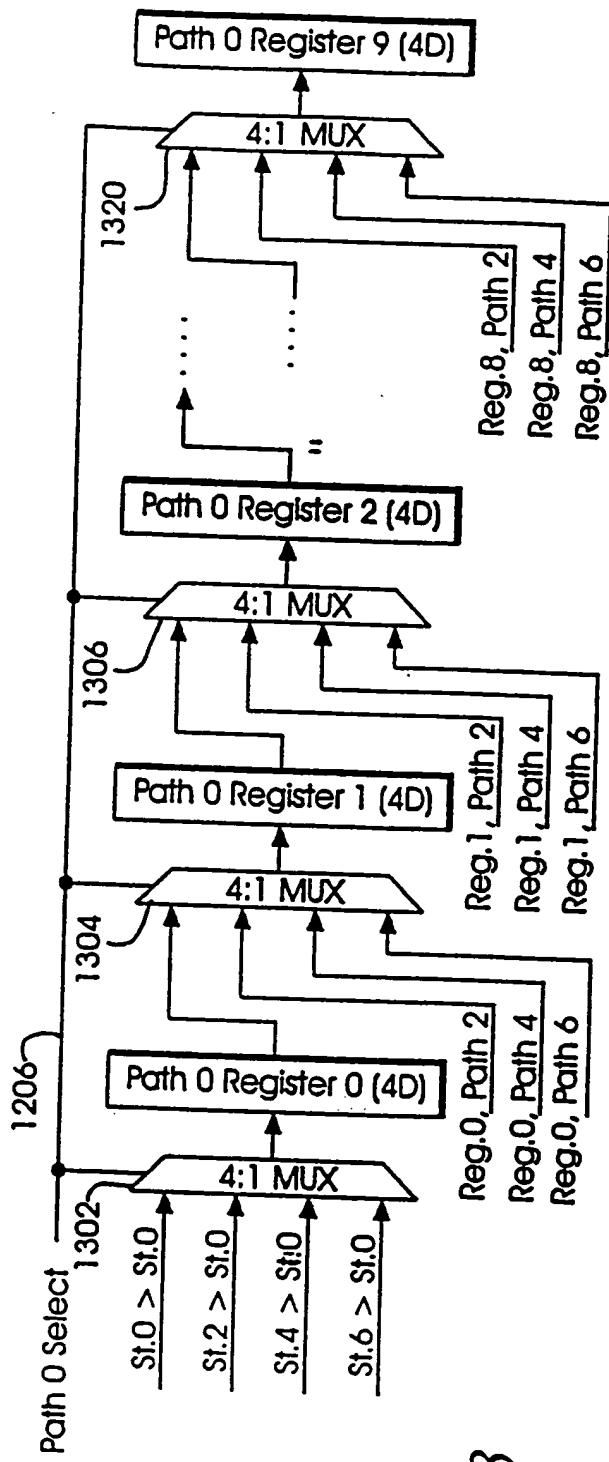


FIG. 13

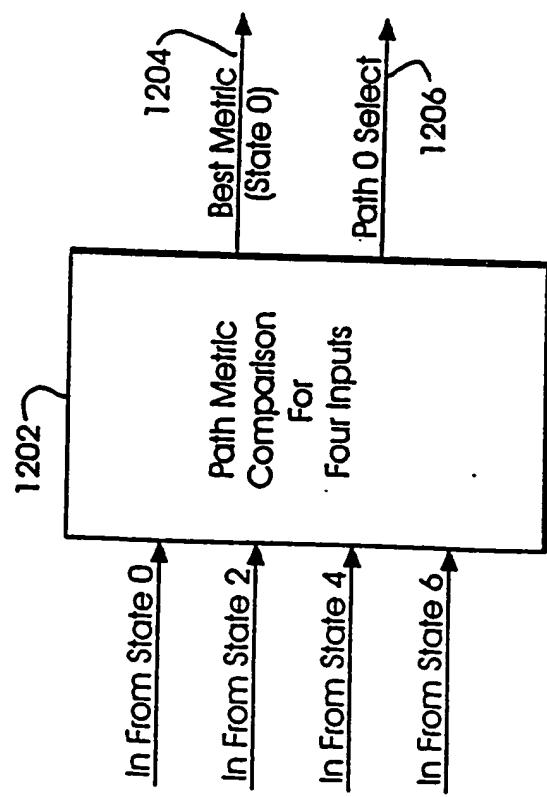


FIG. 12

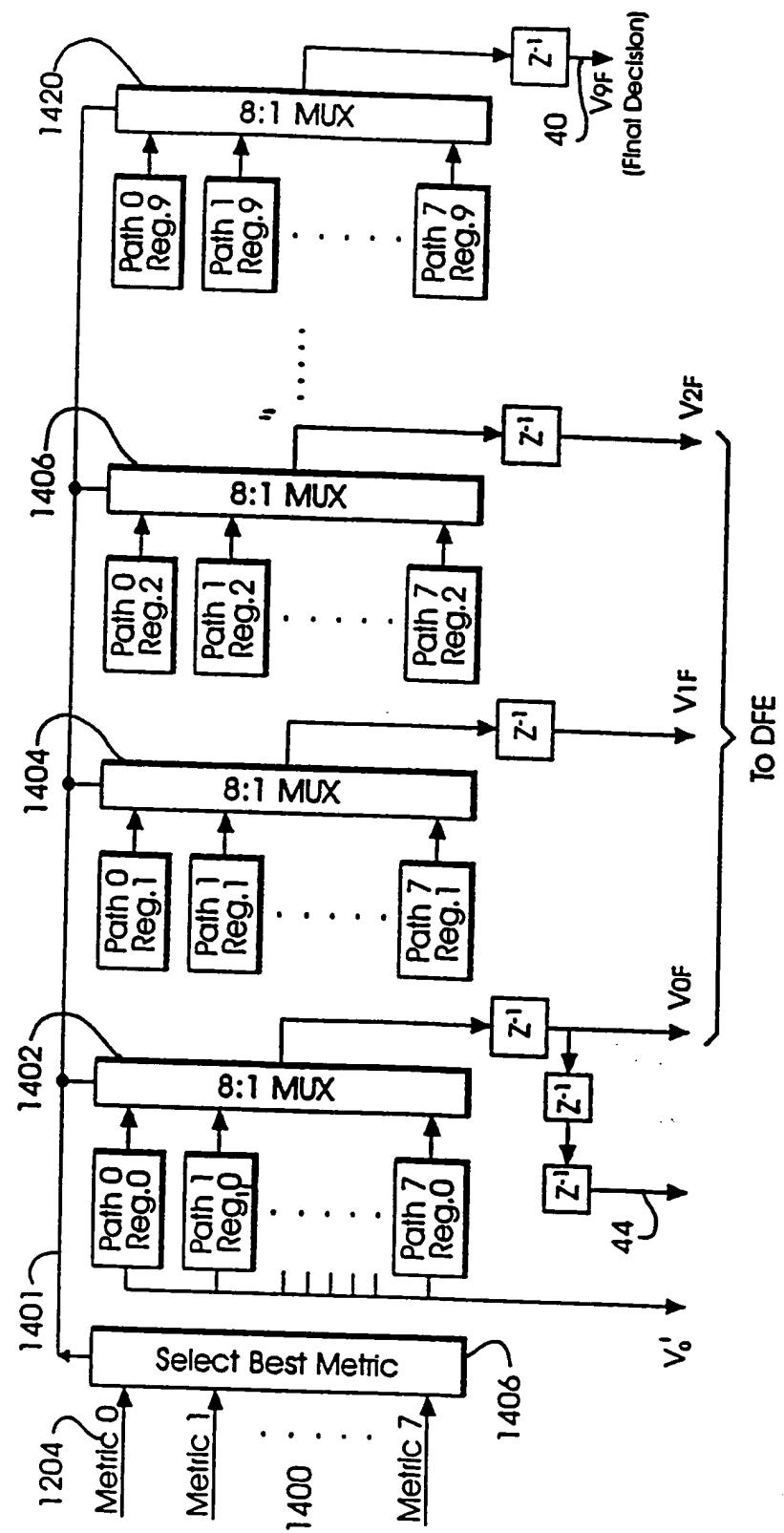


FIG. 14

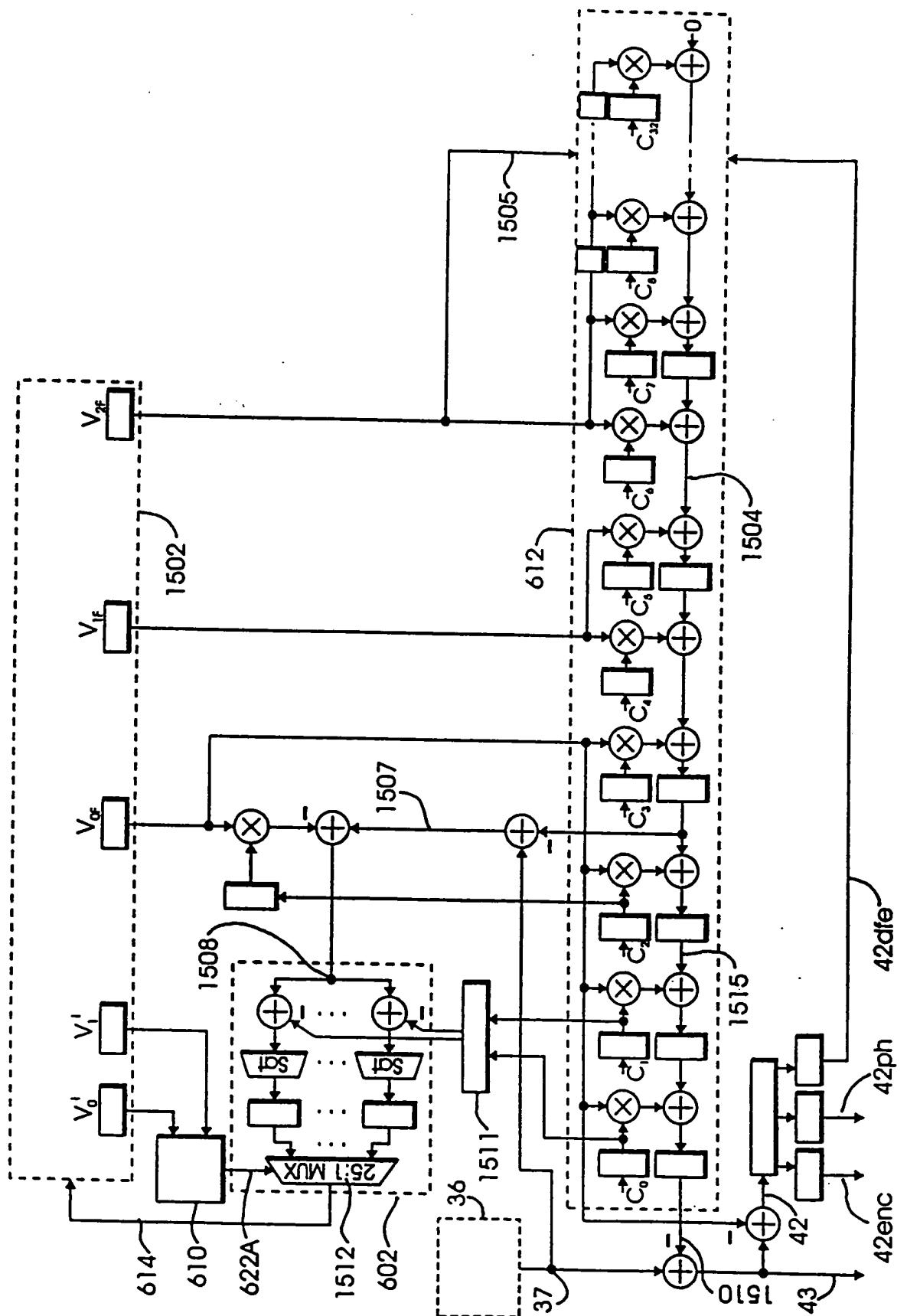


FIG. 15

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Viterbi Input		\$5.3
1D Error		\$4.2
1D Error <sup>2</sup>		U3.2
2D Distance <sup>2</sup>		U3.2
4D Distance <sup>2</sup>		U4.2 Before Min Select
4D Distance <sup>2</sup>		U4.2 After Min Select

*FIG. 16*

Error Values	1D Distance <sup>2</sup> Values
00.00	0.00
00.01 / 11.11	0.00
00.10 / 11.10	0.01
00.11 / 11.01	0.10
01.00 / 11.00	1.00

*FIG. 17*

FIG. 18A

VITERBI INPUT	DECISION X	ERROR X	ROUNDEDERR OR X	ERROR X**2	DECISION Y	ERROR Y	ROUNDEDERR OR Y	ERROR Y**2
01.111	001	00.111	01.00	1.00	010	11.111	00.00	0.00
01.110	001	00.110	00.11	0.10	010	11.110	11.11	0.00
01.101	001	00.101	00.11	0.10	010	11.101	11.11	0.00
01.100	001	00.100	00.10	0.01	010	11.100	11.10	0.01
01.011	001	00.011	00.10	0.01	010	11.011	11.10	0.01
01.010	001	00.010	00.01	0.00	010	11.010	11.01	0.10
01.001	001	00.001	00.01	0.00	010	11.001	11.01	0.10
01.000	001	00.000	00.00	0.00	010	11.000	11.00	1.00
00.111	001	11.111	00.00	0.00	000	00.111	01.00	1.00
00.110	001	11.110	11.11	0.00	000	00.110	00.11	0.10
00.101	001	11.101	11.11	0.00	000	00.101	00.11	0.10
00.100	001	11.100	11.10	0.01	000	00.100	00.10	0.01
00.011	001	11.011	11.10	0.01	000	00.011	00.10	0.01
00.010	001	11.010	11.01	0.10	000	00.010	00.01	0.00
00.001	001	11.001	11.01	0.10	000	00.001	00.01	0.00
00.000	001	11.000	11.00	1.00	000	00.000	00.00	0.00

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FIG. 18B

VITERBI INPUT	DECISION X	ERROR X	ROUNDEDERR OR X	ERROR X**2	DECISION Y	ERROR Y	ROUNDEDERR OR Y	ERROR Y**2
11.111	111	00.111	01.00	1.00	000	11.111	00.00	0.00
11.110	111	00.110	00.11	0.10	000	11.110	11.11	0.00
11.101	111	00.101	00.11	0.10	000	11.101	11.11	0.00
11.100	111	00.100	00.10	0.01	000	11.100	11.10	0.01
11.011	111	00.011	00.10	0.01	000	11.011	11.10	0.01
11.010	111	00.010	00.01	0.00	000	11.010	11.01	0.10
11.001	111	00.001	00.01	0.00	000	11.001	11.01	0.01
11.000	111	00.000	00.00	0.00	000	11.000	11.00	1.00
10.111	111	11.111	00.00	0.00	110	00.111	01.00	1.00
10.110	111	11.110	11.11	0.00	110	00.110	00.11	0.10
10.101	111	11.101	11.11	0.00	110	00.101	00.11	0.10
10.100	111	11.100	11.10	0.01	110	00.100	00.10	0.01
10.011	111	11.011	11.10	0.01	110	00.011	00.10	0.01
10.010	111	11.010	11.01	0.10	110	00.010	00.01	0.00
10.001	111	11.001	11.01	0.10	110	00.001	00.01	0.00
10.000	111	11.000	11.00	1.00	110	00.000	00.00	0.00

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